Refine Search

Search Results -

Terms	Documents
L1 same (interrupt or request)	14

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (interrupt or request)	14	L2
L1	("virtual machine" or VM) same multiplex$3	235	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same (interrupt or request)	14	L2
L1	("virtual machine" or VM) same multiplex$3	235	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(700/1 |710/260 |710/261 |710/262 |710/263 |710/264 |710/265 |710/266 |710/267 |710/268 |710/269 |710/200 |710/40 |710/48 |710/49 |711/6 |711/151 |711/203 |718/1 |718/100 |718/103 |718/108 |712/224 |712/244).ccls.	7623

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	710/260-269,200,40,48,49;712/224,244;718/1,100,103,108;711/6,151,203;700/1.ccls.	7623	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L3	34

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L4	l1 and L3	34	L4
L3	processor same memory same interrupt same ("virtual machine" or VM)	76	L3
L2	L1	7623	L2
L1	710/260-269,200,40,48,49;712/224,244;718/1,100,103,108;711/6,151,203;700/1.ccls.	7623	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
processor same memory same (interrupt near2 request) same ("virtual machine" or VM)	10

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	processor same memory same (interrupt near2 request) same ("virtual machine" or VM)	10	L2
L1	processor same memory same interrupt same ("virtual machine" or VM)	76	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
processor same memory same (interrupt near2 request) same ("virtual machine" or VM)	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, October 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	processor same memory same (interrupt near2 request) same ("virtual machine" or VM)	2	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	processor same memory same (interrupt near2 request) same ("virtual machine" or VM)	10	L2
L1	processor same memory same interrupt same ("virtual machine" or VM)	76	L1

END OF SEARCH HISTORY

Results for "((virtual machine<in>metadata) <and> (interrupt<in>metadata))<and> (p..." e-mail printer friendly

Your search matched **1** of **1250969** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

((virtual machine<in>metadata) <and> (interrupt<in>metadata))<and> (processor

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **Test floor verification of multiprocessor hardware**
   Saha, A.; Lin, J.; Lockett, C.; Malik, N.; Shamsi, U.;
   Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on
   27-29 March 1996 Page(s):373 - 377
   Digital Object Identifier 10.1109/PCCC.1996.493659
   AbstractPlus | Full Text: PDF(476 KB) IEEE CNF

Indexed by Inspec

Test floor verification of multiprocessor hardware

Saha, A. Lin, J. Lockett, C. Malik, N. Shamsi, U.
RISC 6000 Div., IBM, USA

This paper appears in: **Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on**
Publication Date: 27-29 March 1996
On page(s): 373 - 377
Meeting Date: 03/27/1996 - 03/29/1996
Location: Scottsdale, AZ
INSPEC Accession Number:5384976
Digital Object Identifier: 10.1109/PCCC.1996.493659
Posted online: 2002-08-06 20:20:35.0

Abstract
Verification of multiprocessor (MP) system hardware on the test floor for coherence violations is a challenging problem because internal signals are not as readily available as they are in simulation models. Furthermore, in high performance MP systems which employ weak ordering, races between accesses to the same coherence granule can result in non-deterministic results, thereby adding to the difficulty. Therefore, a common verification practice has been to either allow false sharing only or restrict multiple **processors** from accessing the exact same location without using some form of a "barrier" around the shared location. This allows the execution results to be deterministic so that they can be predicted for static checking at the end of the test program. The paper presents a methodology for detecting coherency violations in weakly ordered multiprocessor systems with arbitrary streams of instructions and without restricting the level of sharing by the processors. This verification is performed under the native operating system of the system under test. In our methodology, only a weak relative ordering of instruction issuance and completion times of loads are sufficient. The method ensures that data returned for each different load from the same **processor** is stored in a different register each time until no more new registers are available, at which point a program **interrupt** is generated and the results at that time verified across the system. The test vectors are designed to make full use of the different registers in the system. This technique defines a maximal window during which exact ordering violations are checked. The methodology described here also establishes a process that applies equally well to simulation models as well as floor testing and is 100% portable across the two environments

Index Terms
Inspec

Controlled Indexing
coherence computer testing shared memory systems virtual machines

Non-controlled Indexing
arbitrary instruction streams coherence granule access races coherence violations completion times deterministic execution results exact ordering violations false sharing high performance multiprocessor systems instruction issuance maximal window multiprocessor hardware native operating system program interrupt register shared location simulation models static checking test floor verification test program test vectors weakly ordered

multiprocessor systems

Author Keywords

Not Available

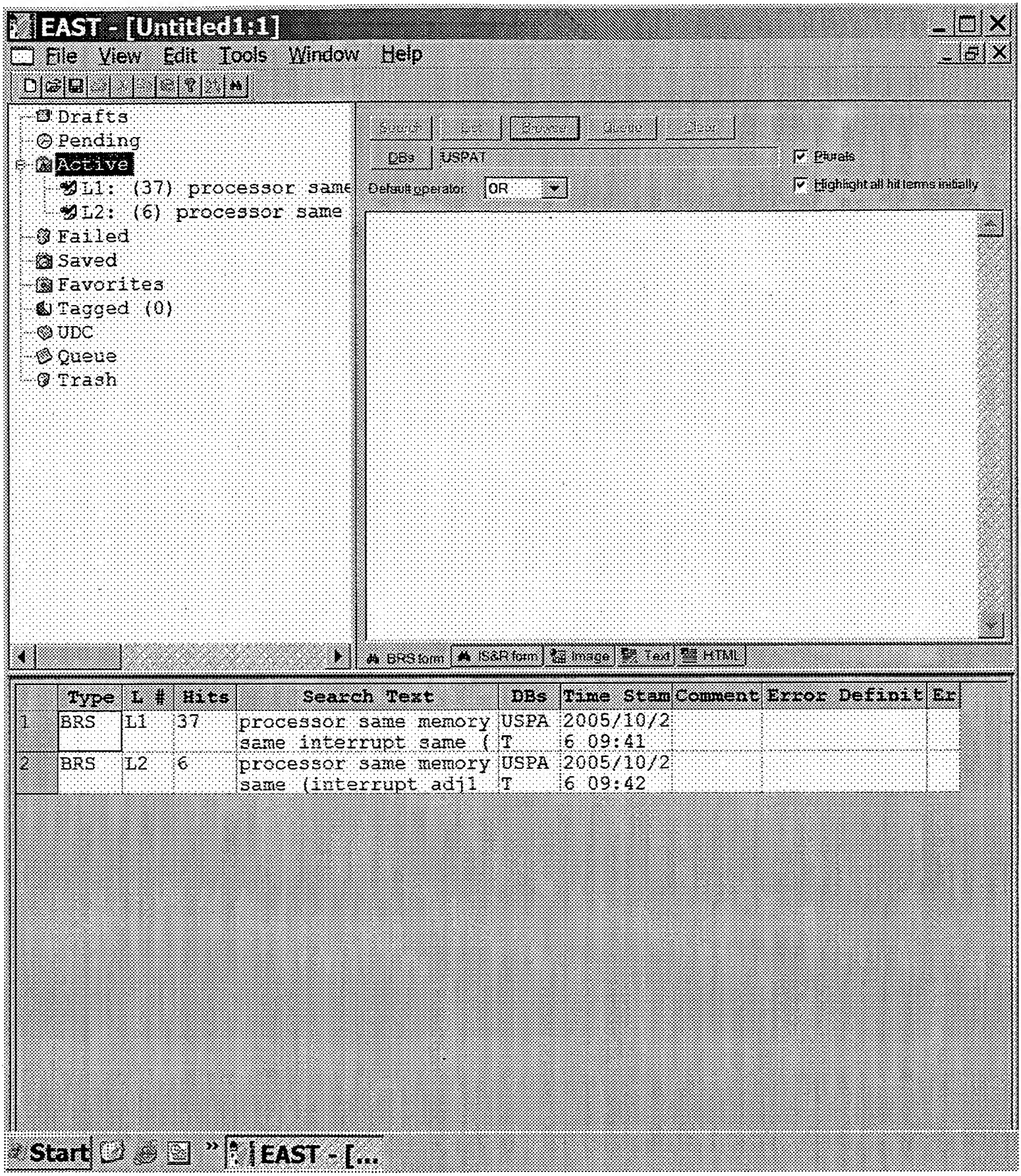
References

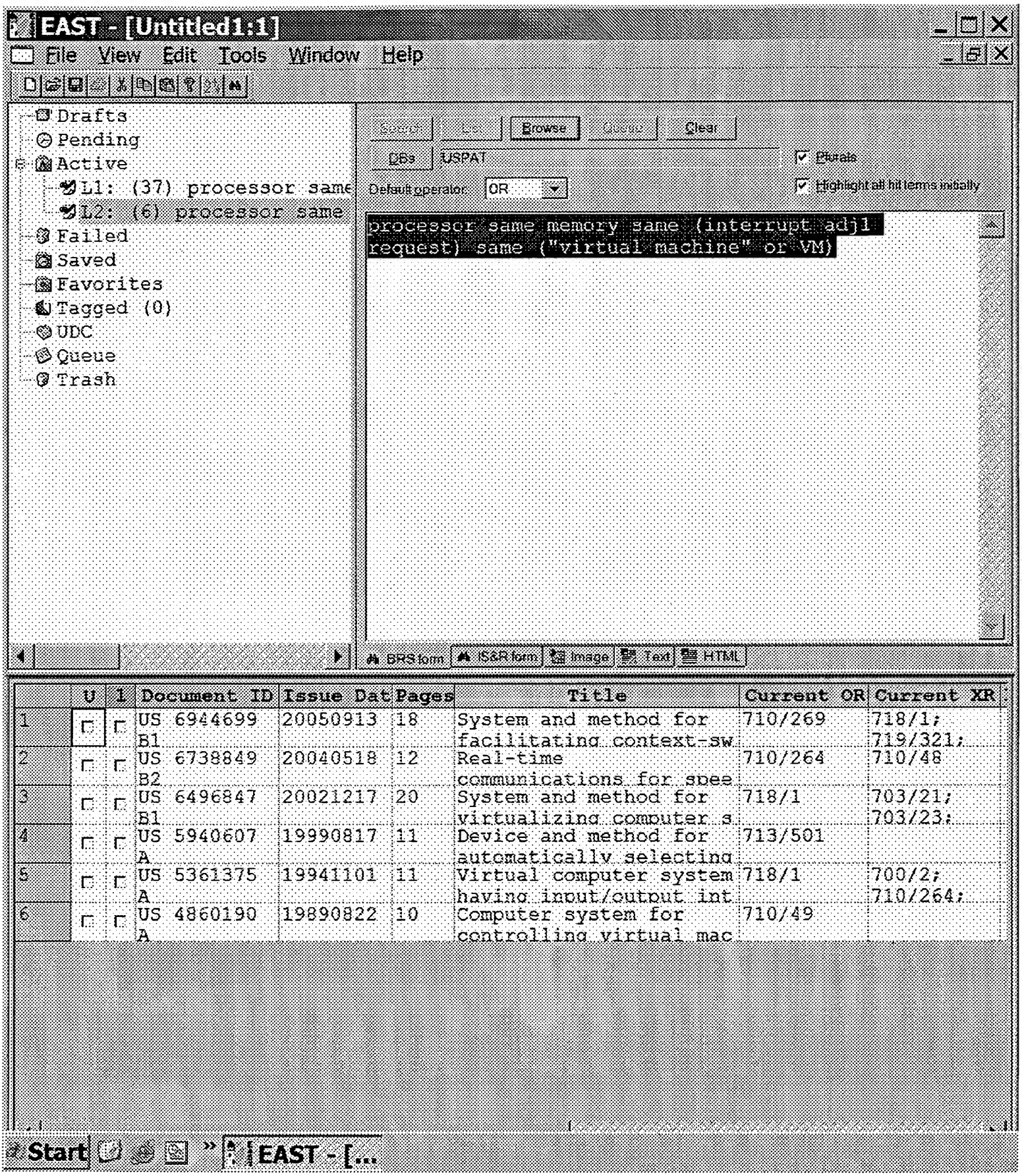
No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

View Search Results


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (37) processor same
L2: (6) processor same
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
Edit
Browse
Queue
Clear
DBs
USPAT
Plurals
Highlight all hit terms initially
Default operator:
OR
BRS form
IS&R form
Image
Text
HTML
Type L # Hits Search Text DBs Time Stam Comment Error Definit Er
1 BRS L1 37 processor same memory same interrupt same (USPA T 2005/10/26 09:41
2 BRS L2 6 processor same memory same (interrupt adj1 USPA T 2005/10/26 09:42
Start
EAST - [...


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (37) processor same
L2: (6) processor same
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
Edit
Browse
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
processor same memory same (interrupt adj1 request) same ("virtual machine" or VM)
BRS form
IS&R form
Image
Text
HTML
U
1
Document ID
Issue Dat
Pages
Title
Current OR
Current XR
1 US 6944699 B1 20050913 18 System and method for facilitating context-sw 710/269 718/1; 719/321;
2 US 6738849 B2 20040518 12 Real-time communications for spee 710/264 710/48
3 US 6496847 B1 20021217 20 System and method for virtualizing computer s 718/1 703/21; 703/23;
4 US 5940607 A 19990817 11 Device and method for automatically selecting 713/501
5 US 5361375 A 19941101 11 Virtual computer system having input/output int 718/1 700/2; 710/264;
6 US 4860190 A 19890822 10 Computer system for controlling virtual mac 710/49
Start
EAST - [...